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10/783,936	02/20/2004	Jack C. Wybenga	2003.07.006.BN0	7287

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DUONG, CHRISTINE T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,936	WYBENGA ET AL.	
	Examiner	Art Unit	
	Christine Duong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

1. **Claims 2-9, 11-23** are objected to because of the following informalities:

Claims 2-9, 11-18, 20-23 recite the limitation "Claim" in Line 1. It is suggested to replaced "Claim" in Line 1 with --claim--.

Regarding **Claim 19**, it is suggested to rewrite "the first routing node" in Line 9 as --a first routing node--.

Regarding **Claim 23**, it is suggested to rewrite "the first external devices" in Line 2 as --the first external device--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1, 3-8, 10, 12-17, 19, 21-23** are rejected under 35 U.S.C. 102(e) as being anticipated by Chapman et al. (PG Pub US 2003/0103450 A1).

It is noted, with respect to **Claims 1, 3, 10, 12** and **21** that the language used by Applicant merely suggests or makes optional those features described as "capable of"; such language does not require steps to be performed nor limits the claim to a particular structure.

It has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchinson, 69 USPQ 138.

Regarding **Claim 1**, Chapman et al. discloses a router for interconnecting external devices coupled to said router **(Figs. 1-3)**, said router comprising:

a switch fabric **(switch fabric 210, Fig. 2)**; and

a plurality of routing nodes coupled to said switch fabric **(interfaces 202, 204, 206, Fig. 2)**, wherein each of said plurality of routing nodes comprises packet processing circuitry capable of transmitting data packets to, and receiving data packets from, said external devices **("the interfaces 202, 204 and 206 interconnect various input and output ports to the physical links 5, 6 and 7, respectively", [0100] Lines 1-3 and "these ports connect the router to physical links 5, 6 and 7, allowing data to be transported to other switches within the network", [0099] Lines 7-9 and further Fig. 2)** and further capable of transmitting data packets to, and receiving data packets from, other ones of said plurality of routing nodes via said switch fabric **("the function of the interface 202 is to transmit incoming data packets to the internal bus 306 for transport to the memory 310 where they can be processed by the processor 308 before being sent over the switch fabric 210. On the output side, the interfaces are designed to accept data packets from the switch fabric 210 and impress the necessary electrical signals over the respective physical links so that the signal transmission can take effect", [0100] Lines 10-17 and further Fig. 2)**,

wherein said switch fabric is capable of detecting that the output bandwidth of a first output of said switch fabric has been exceeded **("the program element then determines the output rate of the queue at step 508 and, at step 510, compares this measured value to the queue's minimum and maximum allocated bandwidth values, as found stored in a configuration table in the memory 310", [0115] Lines 37-41)** and, in response to said detection, said switch fabric causes a first one of said plurality of routing nodes to slow an input rate of data packets transmitted from said first routing node to a first input of said switch fabric **("by independently controlling the transport of data packets on every logical pathway, the aggregate data input rates to the switch fabric can be controlled so as not to exceed the limits of the assigned rates on outgoing links from the switch", [0025] Lines 7-11).**

Regarding **Claim 10**, Chapman et al. discloses similar elements as described above in Claim 1 for each of plurality of routers in a communication network comprising a plurality of routers that communicate data packets to one another and to interfacing external devices **(Figs. 1-3)**.

Regarding **Claims 3** and **12**, Chapman et al. discloses everything claimed as applied above (see *Claims 1* and *10*, respectively). In addition, Chapman et al. discloses said first routing node comprises a first queue comprising a plurality of prioritized buffers capable of storing data packets to be transmitted to said switch fabric **("the processor 308 will dynamically create virtual queues within memory for the traffic for each particular class traveling through the switch fabric on a different logical pathway towards a particular output port ... Specific to the example**

depicted in FIG. 1, interface 202 will have two virtual queue buffers set up in memory 310 as a result of the two different classes of traffic arriving at router D on physical link 5", [0103] Lines 4-12).

Regarding **Claims 4** and **13**, Chapman et al. discloses everything claimed as applied above (see *Claims 3* and *12*, respectively). In addition, Chapman et al. discloses said first routing node slows down a rate at which data packets are transmitted to said switch fabric from said first queue **("by independently controlling the transport of data packets on every logical pathway, the aggregate data input rates to the switch fabric can be controlled so as not to exceed the limits of the assigned rates on outgoing links from the switch", [0025] Lines 15-19).**

Regarding **Claims 5** and **14**, Chapman et al. discloses everything claimed as applied above (see *Claims 4* and *13*, respectively). In addition, Chapman et al. discloses said first routing node selects data packets to be transferred to said switch fabric from a first one of said plurality of prioritized buffers according to a priority value associated with said first prioritized buffer **("the traffic in each queue is accounted for and, as a result, priorities of the different virtual queues are set before making a transmission request of the fabric controller 208. The latter recognizes the different queue priorities and accordingly determines and sets the transmission schedule of data packets being released from the queues to the switch fabric, which finally routes the data packets over their logical pathway to their corresponding output port", [0104] Lines 5-13).**

Regarding **Claims 6** and **15**, Chapman et al. discloses everything claimed as applied above (see *Claims 5* and *14*, respectively). In addition, Chapman et al. discloses said first routing node causes a first one of said external devices to slow a rate at which data packets are transmitted to said first queue **("by independently controlling the transport of data packets on every logical pathway, the aggregate data input rates to the switch fabric can be controlled so as not to exceed the limits of the assigned rates on outgoing links from the switch", [0025] Lines 15-19).**

Regarding **Claims 7** and **16**, Chapman et al. discloses everything claimed as applied above (see *Claims 3* and *12*, respectively). In addition, Chapman et al. discloses said first routing node routes said data packets using Layer 3 routing information **("IP is responsible for transporting packets of data from node to node. It forwards each packet based on a four-byte destination address (IP number)", [0008] Lines 3-6 and further "when a certain data packet is received at an input port, the local controller determines first the destination of the packet. This is done by reading the destination address field of the data packet", [0027] Lines 1-4).**

Regarding **Claims 8** and **17**, Chapman et al. discloses everything claimed as applied above (see *Claims 7* and *16*, respectively). In addition, Chapman et al. discloses said Layer 3 routing information comprises an Internet protocol (IP) address **("IP is responsible for transporting packets of data from node to node. It forwards each packet based on a four-byte destination address (IP number)", [0008] Lines**

3-6 and further "when a certain data packet is received at an input port, the local controller determines first the destination of the packet. This is done by reading the destination address field of the data packet", [0027] Lines 1-4).

Regarding **Claim 19**, Chapman et al. discloses for use in a router **(Figs. 1-3)** comprising a switch fabric **(switch fabric 210, Fig. 2)** and a plurality of routing nodes **(interfaces 202, 204, 206, Fig. 2)**, each of the routing nodes comprising packet processing circuitry for transmitting data packets to, and receiving data packets from, external devices and other routing nodes via the switch fabric **("the interfaces 202, 204 and 206 interconnect various input and output ports to the physical links 5, 6 and 7, respectively", [0100] Lines 1-3 and "these ports connect the router to physical links 5, 6 and 7, allowing data to be transported to other switches within the network", [0099] Lines 7-9 and "the function of the interface 202 is to transmit incoming data packets to the internal bus 306 for transport to the memory 310 where they can be processed by the processor 308 before being sent over the switch fabric 210. On the output side, the interfaces are designed to accept data packets from the switch fabric 210 and impress the necessary electrical signals over the respective physical links so that the signal transmission can take effect", [0100] Lines 10-17 and further Fig. 2)**, a method of routing data packets comprising the steps of:

in the switch fabric, detecting that the output bandwidth of a first output of the switch fabric has been exceeded **("the program element then determines the output rate of the queue at step 508 and, at step 510, compares this measured value to**

the queue's minimum and maximum allocated bandwidth values, as found stored in a configuration table in the memory 310", [0115] Lines 37-41); and

in response to the detection, causing the first routing node to slow an input rate of data packets transmitted from the first routing node to a first input of the switch fabric **("by independently controlling the transport of data packets on every logical pathway, the aggregate data input rates to the switch fabric can be controlled so as not to exceed the limits of the assigned rates on outgoing links from the switch", [0025] Lines 15-19).**

Regarding **Claim 21**, Chapman et al. discloses everything claimed as applied above (see *Claim 19*). In addition, Chapman et al. discloses the first routing node comprises a first queue comprising a plurality of prioritized buffers capable of storing data packets to be transmitted to the switch fabric **("the processor 308 will dynamically create virtual queues within memory for the traffic for each particular class traveling through the switch fabric on a different logical pathway towards a particular output port ... Specific to the example depicted in FIG. 1, interface 202 will have two virtual queue buffers set up in memory 310 as a result of the two different classes of traffic arriving at router D on physical link 5", [0103] Lines 4-12).**

Regarding **Claim 22**, Chapman et al. discloses everything claimed as applied above (see *Claim 21*). In addition, Chapman et al. discloses selecting data packets to be transferred to the switch fabric from a first one of the plurality of prioritized buffers according to a priority value associated with the first prioritized buffer **("the traffic in**

each queue is accounted for and, as a result, priorities of the different virtual queues are set before making a transmission request of the fabric controller 208. The latter recognizes the different queue priorities and accordingly determines and sets the transmission schedule of data packets being released from the queues to the switch fabric, which finally routes the data packets over their logical pathway to their corresponding output port", [0104] Lines 5-13).

Regarding **Claim 23**, Chapman et al. discloses everything claimed as applied above (see *Claim 22*). In addition, Chapman et al. discloses causing the first external devices to slow a rate at which data packets are transmitted to the first queue **("by independently controlling the transport of data packets on every logical pathway, the aggregate data input rates to the switch fabric can be controlled so as not to exceed the limits of the assigned rates on outgoing links from the switch", [0025] Lines 15-19).**

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2, 11** and **20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman et al. further in view of Murakami et al. (PG Pub US 2004/0179542 A1).

Regarding **Claims 2, 11** and **20**, Chapman et al. discloses everything claimed as applied above (see *Claims 1, 10,* and *19*, respectively). However, Chapman et al. fails

to specifically disclose that the switch fabric implements a Weighted Fair Queuing algorithm to slow the input rate of data packets from the first routing node, as claimed.

Nevertheless, Murakami et al. teaches **"in an input and output buffer switch that arranges buffer memories at input and output ports, respectively, the problem of the static occupation of an output circuit by specific connections can be improved by a buffer memory read scheduling criterion such as Weighted Fair Queuing (WFQ)" (Murakami et al.: [0007] Lines 5-10).**

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement a Weighted Fair Queuing algorithm to slow the input rate of data packets from the first routing node because **"a study of buffer memory read scheduling has been actively conducted as one of the techniques that are proposed to provide the QoS guarantee mechanism as mentioned above or a class-based priority control mechanism" (Murakami et al.: [0007] Lines 1-4).**

6. **Claims 9** and **18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman et al. further in view of Gruia (PG Pub US 2002/0135843 A1).

Regarding **Claims 9** and **18**, Chapman et al. discloses everything claimed as applied above (see *Claims 3* and *12*, respectively). However, Chapman et al. fails to specifically disclose that said first routing node routes said data packets using Layer 2 medium access control (MAC) address information, as claimed.

Nevertheless, Gruia teaches **"the switch module is capable of performing layer 2 switching based on MAC addresses" (Gruia: [0051] Lines 13-14).**

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to route data packets using Layer 2 MAC address information because **"the address table provides source and destination addresses for packets that are being forwarded through the switch module" (Gruia: [0051] Lines 9-11).**

Citation of Pertinent Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boduch et al. (PG Pub US 2004/0085967 A1) discloses reserving bandwidth of a given priority using the WWFA for arbitrating bandwidth among virtual links between input and output ports, each virtual link supporting one of more priorities and corresponding to an arbitration unit (AU) of the WWFA.

Jones et al. (PG Pub US 2003/0058802 A1) discloses determining the data transmission or sending rates in a router or switch of two or more input queues in one or more input ports sharing an output port, which may optionally include an output queue. The output port receives desired or requested data from each input queue sharing the output port. The output port analyzes this data and sends feedback to each input port so that, if needed, the input port can adjust its transmission or sending rate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Duong whose telephone number is (571) 270-1664. The examiner can normally be reached on Monday - Friday: 830 AM-6 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CTD 07/30/2007 CTD

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